Supporting Information:

Metal-Insulator-Semiconductor Nanowire Network Solar Cells

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Methods:

Fabrication:

To isolate the effect of the metal nanowire network on the MIS solar cell performance, we are using a state-of-the-art contact scheme for the back of the solar cell, which is employed in industrial solar cells (see Fig. 1). This half cell consists of a double side polished float zone silicon base wafer with low n-type doping (3 Ωcm), followed by different layers which create the back contact; a thin film of intrinsic hydrogenated amorphous silicon (a-Si:H) (5 nm) followed by a layer of highly doped n-type a-Si:H (8 nm) are grown on the silicon wafer by plasma enhanced chemical vapor deposition (PECVD, Roth & Rau). The n-type a-Si:H is contacted via a sputtered indium tin oxide (ITO) layer (80 nm), followed by a sputtered silver layer (300 nm) as metal contact (Roth & Rau AK tool system).

The passivating and insulating layer, which is grown on the front surface after a short HF treatment (45 s in 1%), consists of 3 nm intrinsic a-Si:H followed by 1 nm of Al_2O_3.[9] The a-Si:H is grown by inductively coupled plasma chemical vapor deposition (ICP-CVD, PlasmaLab System 100, Oxford Instruments) and is used due to the excellent chemical passivation properties on the silicon surface.[10] An argon and silane flow of 20 sccm, a temperature of 50 °C and a power of 400 W at a pressure of 10 mTorr were used for 24 s (~3 nm thickness). The Al_2O_3 layer (9 cycles with a total nominal thickness of ~1 nm) is grown by atomic layer deposition (ALD) (OpAL, Oxford Instruments) at 190 C with TMA and O2 plasma. Al_2O_3 is known for its high stability and insulating properties. When used directly on silicon, ALD-Al_2O_3 has been shown to exhibits a high fixed charge density, which can lead to a field effect passivation of the underlying surface.[11–14] Subsequently, the samples were exposed to N_2 atmosphere in a rapid thermal annealing oven at 190C for 30 min.

The passivated and back contacted half cells were fabricated on 4 inch wafers, which were subsequently cut into about 2-3 cm^2 small pieces to allow the optimization of the following fabrication steps.

The square metal network (nanowire width ~ 100 nm, network pitch ~ 1-2 µm) is fabricated by electron beam lithography (EBL) on small areas (2.4 – 4.5 mm^2) on ~2 cm^2 substrates. EBL resist ZEP 520 A (Zeonrex Electronic Chemicals) is used in a 2:1 mixture with anisole and spun (1000 rpm for 40s) to achieve a resist thickness of ~ 200 nm. Afterwards, the substrates are baked at 180 °C for 5 min. The resist is exposed with 30 kV beam acceleration at a dose of 400 µC/cm^2 (10 µm aperture) in a fixed beam-moving stage modus (FBMS), with a predefined square nanowire network structure with pitches of 1 µm and 2 µm. After developing in pentylacetate for 1 min the samples are rinsed for 15 s in a 9:1 mixture of methyl isobutyl ketone (MIBK) and isopropanol (IPA) and additionally for 15 s in pure IPA.

The samples are blow-dried with nitrogen and transferred to the vacuum chamber of an electron beam evaporator. At a pressure of ~ $5x10^{-7}$ mbar, first a 10 nm thin layer of palladium, followed by a 40 nm thin layer of gold are evaporated at a rate of 0.2 - 0.5

Å/s out of a water-cooled copper and a tungsten crucible, respectively. The Pd and the Au pellets are of at least 99.95% purity.

This double structure is used because of the higher work function (WF) of Pd (5.2 - 5.6 eV) than Au (5.1 - 5.5 eV), which allows a stronger inversion in the underlying silicon, and the lower optical losses of Au compared to Pd.

After the evaporation, the samples are immersed in warm acetone (50 °C) to dissolve the EBL resist and this way lift-off the redundant metal film, leaving behind the desired square metal nanowire network structure.

Metal pads for later contacting purposes are placed on two sides of the square network with conventional UV lithography and subsequent metal evaporation, using a 100 nm, opaque Au layer.

Electron beam (e-beam) and intense UV light exposure is known to cause damage in a-Si:H. Therefore, the samples are subsequently transferred into a vacuum oven and annealed for 60 min at a pressure of $5x10^{-5}$ mbar and a temperature of 220 °C to reverse the majority of the damage (see Fig. S10).

The integrated inverted nanopyramids in between the metal nanowire network were fabricated by first fabricating the metal nanowire network on a simple silicon wafer and subsequently immersing the sample into KOH etching solution (30%) for 2 min. at a temperature of 20 °C. The metal (Pd/Au) nanowire network acts as an etching mask for the KOH solution and allows therefore the crystal plane selective dissolution of silicon, with the (111) crystal plane having the slowest etch rate.

Electrical and optical characterization:

The J-V traces of the fabricated solar cells are measured under a solar simulator (Oriel SOL2 94062A (6X6) Class ABA, Newport) with the AM1.5G spectrum at 1 sun (100 mW/cm^2) illumination intensity, under masked conditions and at a temperature of 50 °C. The lamp intensity of the solar simulator is adjusted with a silicon reference cell. The right masking conditions are a crucial step for our solar cells, as the network only covers a small part (2 – 4.5 mm^2) of the passivated silicon half cells (2-3 cm^2 small substrates) (see **Fig. S1**). Electrical probes are used to contact the front pad of the nanowire network and the back contact of the whole substrate with a source measure unit (Agilent B2910). The voltage is scanned with a positive and negative scan rate between -1 and 1V in 2001 steps while the current is being measured. No pronounced hysteresis or instability could be detected during the course of the measurements.

A lifetime of 1 ms was measured on the back contacted (w/o ITO) and front passivated silicon wafers before the nanowire network fabrication with a Sinton WCT-120TS lifetime tester.

The reflection measurements are performed using an integrating sphere setup. A supercontinuum white light source (Fianium) is used to illuminate the solar cells. The

unpolarized light is weakly focused on the back plane of the sphere (4 inch Labsphere) to ensure near to normal incidence. A 105 µm core fiber is used to collect the reflected light and send it to a spectrometer, consisting of a spectrograph (Spectrapro 2300i) and a Si CCD array (PIXIS 400 CCD, cooled to -70 ^{o}C). The measurements cover the 420-970 nm spectral range, and a 400 ms integration time with 50 accumulations were used.

Simulations:

The band diagram simulations are performed with the software package AFORS-HET.[1] The simulated structure consists of an *n*-type Si wafer with a base doping of 1.6×10^{15} cm^{-3}, a 3nm intrinsic a-Si:H layer, a 1 nm Al_2O_3 layer and a metal contact which is simulated by having a fixed work function as boundary condition. Fixed charge is placed at the a-Si:H/Al_2O_3 interface. For the material properties, the default simulation values provided by AFORS-HET are used. Simulations are performed in the dark.

The finite difference time domain (FDTD) simulations are performed with the software package Lumerical to obtain the reflection values for the 80 nm silicon nitride coated (*n*=2) network with and without integrated inverted nanopyramids. The network has a pitch of 1 µm, a nanowire width of 100 nm and a thickness of 50 nm, with 40 nm of Au (top) and 10 nm Pd (bottom). A plane wave (λ = 400 nm – 1100 nm) under normal incidence and a power monitor, positioned above the nanowire network, are used to determine the reflectance. A perfectly matched layer as boundary condition in vertical direction is used to prevent scattering artifacts from the edges of the simulation box, while periodic boundary conditions are used for the in-plane dimensions to simulate an infinite network. The mesh size was 2 nm and the optical constants for Au, Pd and Si are taken from Palik.

Masked measurements and the influence of a small active area fabricated on a large substrate:

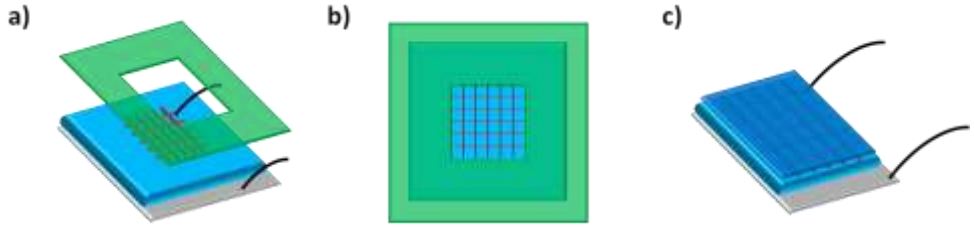

Figure S1: (a), (b) The measurements under illumination are done with a mask (green), which covers the areas of the passivated and back contacted silicon substrate (blue). The mask has an opening in the middle, which allows illumination of the area with the fabricated metal nanowire network (red). (c) The measured V_{oc} is strongly affected by the relatively larger contribution of J_0 compared to J_L. Therefore, the effect is investigated and an effective V_{oc} derived, which allows the estimation of the solar cell performance, for which the substrate has the same size as the active area, as depicted here.

In the following, we investigate the effect of the small size (2.4 - 4.5 mm^2) of the illuminated and with the nanowire network patterned area compared to the large silicon substrate on the open-circuit voltage.

Taking into account that J_0 stems from a much larger region than the photocurrent, we are able to estimate the open-circuit voltage for a 1 cm^2 sample

~~(SI)~~. This way we are able to evaluate and compare our results with regard to other solar cell device architectures and to correct for any effects particular to our sample size and masking conditions.

We use two approaches, based on two separate sets of measurements, that both yield the same result for the estimated V_{oc}.

The first approach investigates the scaling behavior of the recombination parameter J_0 with different sizes of the illuminated and with the metal nanowire network patterned area.

The second approach investigates the variation of the V_{oc} for two different measurements; under masked and under unmasked conditions. This second approach makes use of the fact, that the V_{oc} can be related to the carrier concentration inside the solar cell (implied V_{oc}).[2]

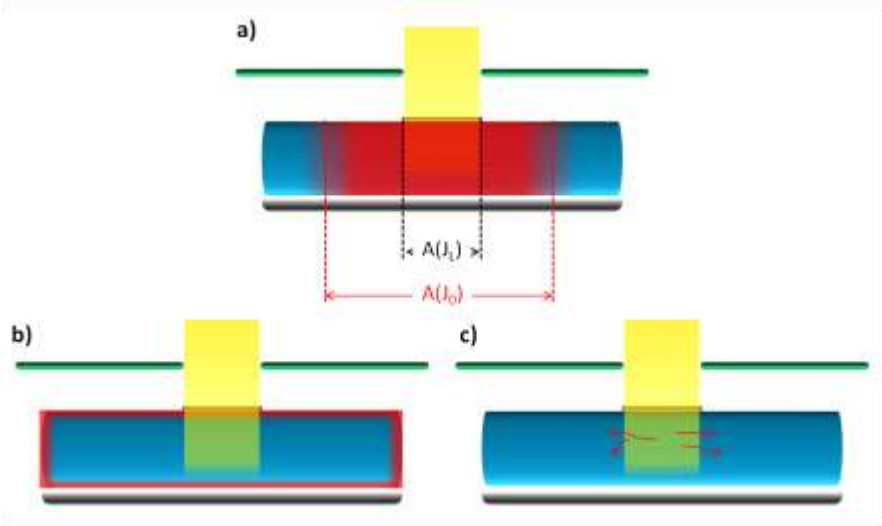

Figure S2: (a) J_0 originates from a larger region than J_L and this way strongly affects the carrier concentration/ quasi-Fermi level splitting in the semiconductor and hence the V_{oc}. (b) As described in the text, the larger J_0 contribution (red) can mainly be attributed to surface recombination and hence be accounted for by investigating the scaling behavior of J_0 with different area size. (c) Another description with the same result can be undertaken by considering the decrease in carrier concentration due to lateral diffusion into the shaded bulk and to the surfaces of the substrate, where recombination can take place. Investigating the V_{oc} variation for different measurement conditions (masked/unmasked) allows the estimation of the V_{oc} for a 1 cm^2 sample.

Due to the results shown below and the nature of our samples, i.e. high-purity monocrystalline FZ-silicon base wafers, we attribute the main contribution to J_0 to recombination active surface sides. This surface recombination and minor contributions from the other recombination processes stem mostly from a larger area than the illuminated one. They are facilitated via diffusion of carriers to unilluminated regions and further to respective recombination sides. This diffusion is therefore partly taking place, because of the difference in the carrier concentrations between the illuminated and the dark regions, which results in a lateral gradient and hence driving force for the charge

carriers away from the illuminated region. The charge carriers can now simply recombine in the dark (mainly band-to-band and SRH recombination) or are further driven towards the surfaces, with the latter being a further cause for an additional gradient in carrier concentrations. Hence, the resulting gradient landscape can be approximated as a lateral gradient, due to a difference in carrier concentrations in the dark and in the light, with a superimposed vertical gradient due to surface recombination.

We note that, because of the importance of those diffusive currents to the recombination processes, the internal current flows under illumination, even for V_{oc} conditions with a total zero net current, are very different from the situation in thermal equilibrium (in the dark). In thermal and chemical equilibrium, i.e. for a solar cell in the dark with open end-terminals, there cannot be any net external current flow and furthermore no internal carrier flow across regions of the solar cell. The principle of detailed balance requires then that recombination currents are matched by thermal generation currents locally, not globally. In the dark, for every recombination current there exists the reverse thermal generation current, e.g. for a local surface recombination current there exists as well a local thermal surface generation current.

In the light, especially diffusive processes due to differences in photo-generated charge carrier concentrations are changing the physical picture. For further explanations, the reader is referred to the excellent publication by *A. Cuevas* about the recombination parameter J_0.[3]

Scaling behavior of J_0 with area size

We compare three samples (S1-S3), that are fabricated in the exact same way, the only difference being the different sizes (2.4 - 4.5 mm^2) of the metal nanowire network (and hence the illuminated area) during illumination. The recombination parameter J_0 is a nontrivial parameter and cannot a priori be ascribed to any particular dimension. As we will discuss in the following, J_0 is mainly originating from surface recombination. However, assuming that J_0 is originating from the whole substrate area would be an oversimplification. Under illumination, the diffusion of photo-generated charge carriers to those recombination active sides has to be taken into account and hence forbids any simple estimation of the contribution of any single dimension or region (e.g. the whole substrate area) to the recombination current.

On the other hand, using three samples, that have been fabricated under the exact same conditions, but are of different size, and investigating the scaling behavior of the recombination current density J_0, we are able to estimate the value of J_0 for a standardized sample size of 1 cm^2 for which the illuminated and the substrate area have the same size. The fact that the short-current density for 1 sun illumination is approximately the same for all the fabricated samples, strongly supports the reproducibility of our fabrication scheme.

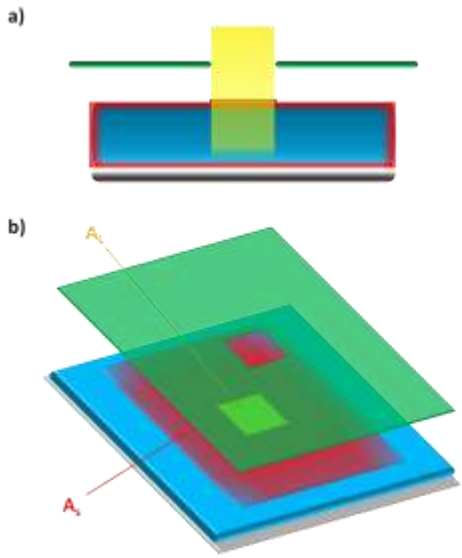

Figure S3: (a) The main contribution to J_0 is originating from surface recombination, as derived and described in the text. (b) The illuminated area A_L is much smaller than the area A_S, which significantly contributes to the recombination current density J_0.

The ideal diode equation results in the well-known V_{oc} equation:[2]

$$V_{oc} = \frac{n * KT}{q} \ln\left(\frac{J_L}{J_0} + 1\right) \sim \frac{n * KT}{q} \ln\left(\frac{J_L}{J_0}\right)$$

with the ideality factor n, the Boltzmann constant K, temperature T (in Kelvin), the elementary charge q, the photocurrent density J_L and the recombination current density J_0.

In the following, we assume an ideality factor of n=1. That assumption doesn't have any influence on our final results for the estimated V_{oc} of a 1cm^2 large sample. It only influences the magnitude of the calculated J_0 values for the differently sized samples (larger J_0 for n>1), not the relative change among them. Due to the exact same fabrication parameters we can assume the same ideality factor for all the samples, including the 1 cm^2 one. So a larger estimated J_0 for the 1 cm^2 sample (due to a n>1) would still result in the same V_{oc} as in the case of n=1, because of the proportional increase of the estimated V_{oc} with the ideality factor (for a constant J_0), as shown below.

Using the above equation, we calculate the recombination parameter J_0 for the three differently sized samples under illumination, using the temperature during measurements of T ~ 50 °C (323 K) and the respective measured V_{oc} and J_{sc} values (see **Table S1**):

$$J_0 = e^{-\frac{V_{oc}}{27.8\ mV}} * J_L$$

$$J_0^{S1} = 6.60 * 10^{-9}\ A/cm^2$$
$$J_0^{S2} = 2.90 * 10^{-9}\ A/cm^2$$
$$J_0^{S3} = 1.68 * 10^{-9}\ A/cm^2$$

In general, J_0^{Total} can be expressed as the sum of the different recombination processes:[3]

$$J_0^{Total} = J_0^{Surf} + J_0^{SRH} + J_0^{Auger} + J_0^{Rad} + \cdots$$

J_0^{Surf} stems from surface recombination, J_0^{SRH} from Shockley-Read-Hall (SRH) recombination, J_0^{Auger} from Auger recombination and J_0^{Rad} from radiative/ band-to-band recombination. Often, J_0^{Total} is also separated according to the different regions in the solar cell from which the respective J_0 originates (e.g. for a n^+-emitter: $J_0^{n^+}$).

As mentioned above, we expect the main contributor to be J_0^{Surf}, due to the absence of highly doped silicon regions and the high crystal quality and purity of the FZ-silicon base wafer.

For our small samples we expect approximately a $1/A_i$ dependency for the J_0, especially with increasing area size up to 1 cm^2, as the total recombination current I_0^{total} can be approximated as a constant, that originates from a much larger area (for surface recombination) or volume (for SRH and Auger).

$$J_0^{S_i}(A_i) = \frac{I_0^{total}}{A_i}$$

The larger area is not necessarily 1 cm^2, but the resulting I_0 will be close to the one expected for such an area, considering the 1/A dependency of the J_0. For increasing area size, but with A_i < 1 cm^2, $J_0^{S_i}(A_i)$ approaches more accurately a value that represents the recombination originating from a 1 cm^2 sample.

However, for the measured small area samples we expect a deviation from the 1/A dependency, due to the nature of our samples. As we show in Fig. S10, we observe electron-beam-induced damage in the top 3 nm a-Si:H layer, which can mostly be removed with a post fabrication anneal. However, as we discuss below, we aren't able to remove all the induced damage, which can be seen for example from the increasing I_{sc} with increasing annealing temperature. We choose an annealing temperature, that is optimized with regard to the V_{oc}, but we can't prove that this maximum V_{oc} is completely unaffected by the damage. As a result, we expect a slightly higher J_0 for the fabricated samples, than a simple 1/A dependency would suggest. However, even for those samples the major J_0 contribution will stem from a much larger area than the illuminated one, unrelated to the electron beam induced degradation.

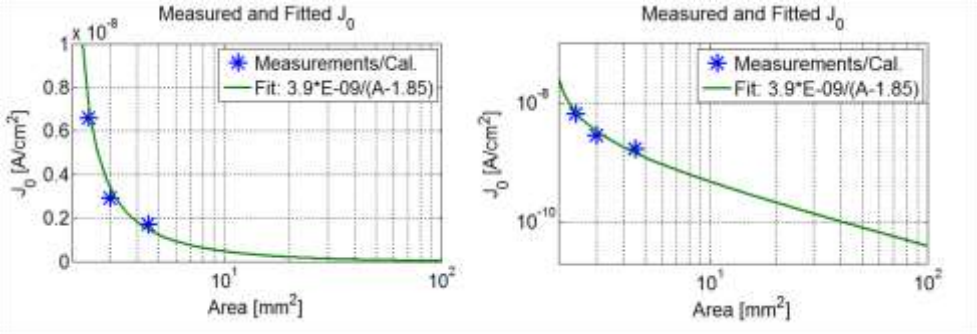

Figure S4: Calculated J_0 values for fabricated small area samples (blue markers) as a function of the area size. Due to reasons described in the text, the J_0 dependency on the area size was fitted with the function 3.9E-09/(A-1.85) (green line). The left and the right graph show the same data, however on semi-log and log-log plots.

Because of those reason, we use a least squares fit method, to fit an equation of the following form to our calculated J_0 values.

$$f(x) = \frac{p}{x+q}$$

As shown in **Fig. S4**, we obtain a good agreement with p=3.90E-09 and q=-1.85:

$$J_0^{S_x} \sim \frac{3.90 * 10^{-9}}{A_x - 1.85}\ A/cm^2$$

Therefore, we can estimate the recombination parameter J_0^{Sa} for a 1 cm^2 large sample:

$$J_0^{Sa} = 3.97 * 10^{-11} A/cm^2$$

Finally, we can calculate the V_{oc} of the 1 cm^2 sample S_a, assuming the short-circuit current density as observed for samples S1 and S3, i.e. ~ 23.2 mA/cm^2. As discussed above, setting the ideality factor n=1 doesn't influence our result, as the estimated J_0^{Sa} would have been higher for 2>n>1.

$$V_{oc}^{S_a} \sim\ n * 27.8\ mV * \ln\left(\frac{J_L^{S_a}}{J_0^{S_a}}\right), \qquad n = 1, \qquad J_L^{S_a} = J_L^{S_1}$$

$$\boldsymbol{V_{oc}^{S_a} \sim 562\ mV}$$

Table S1: Measured (M), calculated (C), estimated (E) and fitted (F) solar cell parameters of the small area samples S1-S3 and the estimated 1 cm^2 sample $S_{a\text{-}1}$.

Sample	**Area**	V_{oc}	J_{sc}	J_0
S1	2.4 mm²	419 mV **(M)**	23.2 mA/cm² **(M)**	660E-11 A/cm² **(C)**
S2	3 mm²	439 mV **(M)**	21.0 mA/cm² **(M)**	290E-11 A/cm² **(C)**
S3	4.5 mm²	457 mV **(M)**	23.3 mA/cm² **(M)**	168E-11 A/cm² **(C)**
$S_{a\text{-}1}$	100 mm²	**562 mV (C)**	23.2 mA/cm² **(E)**	3.97E-11 A/cm² **(F)**

Variation of the V_{oc} for masked and unmasked measurements at 1 sun

The second approach to investigate the effect of the small sample area on the V_{oc} makes use of the fact, that the V_{oc} is related to the carrier concentrations:[2]

$$V_{oc}^{imp} = k_B T * \ln\left(\frac{(N_A + \Delta n)\Delta n}{n_i^2}\right)$$

N_A is the doping concentration, Δn is the excess and n_i the intrinsic carrier concentration. V_{oc}^{imp} is called the implied V_{oc}, because it can be seen as the V_{oc} that is implied/ potentially reachable by the carrier concentrations inside the semiconductor. For the actual V_{oc} the energy levels of the contacts for the charge carrier extraction have to be considered as well. By comparing measurements under illumination of a masked and an unmasked sample, we show that the carrier concentration for the masked sample is the limiting case. The energy levels of the contacts, determined by the metal WF for the (MIS) hole contact and the a-Si:H n-type doping for the electron contact, allow for a substantially higher V_{oc}, than obtained for the masked sample.

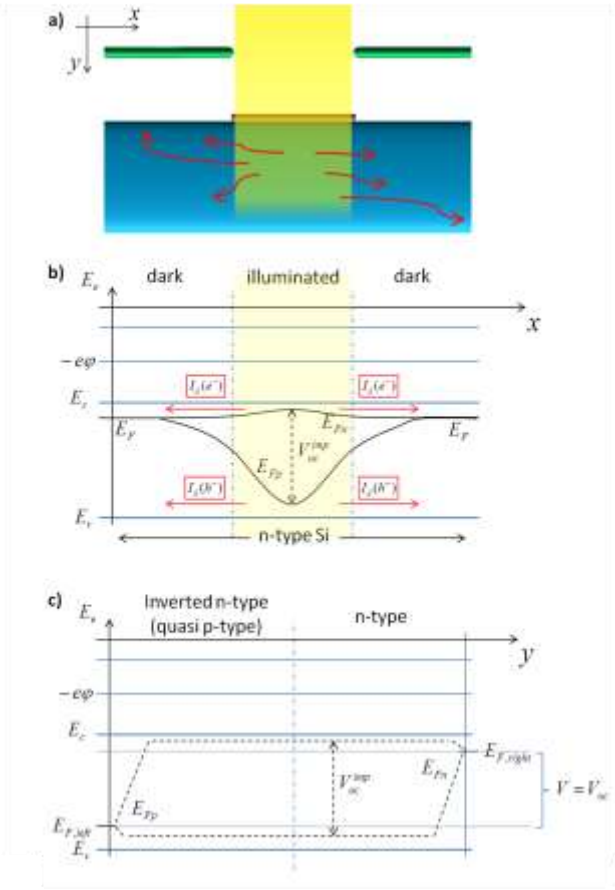

Figure S5: (a) The influence of a smaller illuminated area compared to the substrate can be described by diffusive currents (red arrows) into dark regions and towards recombination active sides. (b) Differences in carrier concentrations between the illuminated and the dark regions inside the bulk n-type wafer lead to gradients in the quasi-Fermi levels, which in turn result in diffusive transport (red arrows) away from the illuminated region. This results in a lower implied V_{oc}. (c) Band diagram under illumination for a typical p(inverted n)-n junction of a solar cell. As can be seen in the figure, in general the implied V_{oc} can be higher than the actual V_{oc}. The diagram neglects the lowering of the implied V_{oc} due to the diffusion of minority charge carriers into the "wrong direction", i.e. to the majority carrier contact where recombination can take place.

Using an illuminated and with a nanowire network patterned area that is smaller than the silicon substrate leads to diffusive lateral current flows, due to the gradient in carrier concentrations away from the illuminated (n*p) towards the dark areas (n*p=n_i^2 for regions far away from the illuminated area). Additional gradients are created because of recombination active sides, such as the surfaces, as discussed above.

As shown in **Fig. S5**, the lateral diffuse currents $I_d(h^+)$ and $I_d(e^-)$ towards the dark regions lead to a decrease in the carrier concentrations in the small illuminated region. This decrease directly results in a decrease in the quasi-Fermi level splitting, i.e. V_{oc}^{imp}. V_{oc}^{imp} is hence lower, than it would be for a completely illuminated substrate, for which only gradients in the carrier concentrations due to the surface recombination exist. However, the interpretation of an unmasked measurement for which the complete substrate is illuminated has to be done with caution.

First of all, only a small part of the area that is illuminated is also patterned with the nanowire network. As shown in Fig. 4, the optical properties of the flat metal nanowire network on top of silicon are very similar to a flat bare silicon substrate (36 vs. 33 % reflection, and 10% additional absorption).

However, because of the logarithmic dependence of the V_{oc} on the I_{sc}, the overestimation ($V_{oc}^{S_1 optical}$) due to the slightly lower reflection of the bare silicon wafer and the absence of metal absorption can be neglected:

$$\Delta V_{oc}^{diff} = V_{oc}^{S_1 nomask} - V_{oc}^{S_1 optical} - V_{oc}^{S_1 mask} \sim 100\ mV$$

$\boldsymbol{V_{oc}^{diff}}$: V_{oc}-loss due to lateral diffusion

$\boldsymbol{V_{oc}^{S_1 optical}}$: V_{oc} – overestimation due to lower reflection of bare silicon surface and absence of metal absorption

$$V_{oc}^{S_1 optical} \sim 0\ \text{mV}$$

$\boldsymbol{V_{oc}^{nomask}}$: $V_{oc}\ of\ unmasked\ sample$

$$\boldsymbol{V_{oc}^{masked}}: V_{oc}\ of\ masked\ sample$$

Sample	Area	V_{oc}	I_{sc}	I-Factor	I_0
S1 (masked)	2.4 mm²	419 mV	0.557 mA	-	
S1 (unmasked)	Unknown (~25 mm²)	519 mV	5.580 mA	1	$I_0^{S_1^{unm}}$
$S_{a\text{-}2}$	100 mm²	**559 mV (C)**	23.3 mA (E)	4.17	$I_0^{S_{x2}} \sim I_0^{S_1^{unm}}$

Table S2: Measured solar cell parameters of the small area sample S1 with and without a shadow mask. Calculated (C) and estimated (E) parameters for the 1 cm^2 sample $S_{a\text{-}2}$

Furthermore, the I_{sc} of the unmasked sample is substantially higher than for the masked sample, especially for high purity silicon with large minority carrier diffusion lengths, but doesn't reach the I_{sc} values predicted for a 1 cm² sample, i.e. 23 mA. For our measurement the unmasked I_{sc} is about 10 times higher than the masked one, i.e. 5.58 mA vs. 0.557 mA, as shown in SI Table 2. We can estimate the area to be roughly 10 times larger than the 2.4 mm^2 small sample (neglecting the slightly different optical properties). Taking into account that the recombination current I_0 for a 24 mm^2 area will be close to the value for a 100 mm^2 (see also the extensive discussion above) we can estimate the additional gain in V_{oc} for a 100 mm^2 sample due to an increase of I_{sc} to 23 mA, with the term ΔV_{oc}^{light}. We note, that the actual I_0 value will be somewhat lower for a 1 cm^2 sample than assumed here, hence this approximation leads to a conservative estimate of the additional V_{oc} gain.

$$\Delta V_{oc}^{light} = 27.8\,mV * \ln(4.17) \approx 40\text{mV}$$

We note, that besides the conservative estimate of the actual I_0 value as described above, an additional deviation is expected due to the less efficient carrier extraction in the case of the unmasked sample, which heavily impacts the fill factor of the unmasked solar cells. The current of 5.58 mA of the unmasked sample is separated and collected with the same inversion layer and metal nanowire network than the 0.557 mA of the masked sample.

Finally, we can estimate the V_{oc} for a 1 cm^2 sample:

$$\mathbf{V_{oc}^{S_{x2}} = V_{oc}^{S_1 mask} + \Delta V_{oc}^{light}(I_0^{S_{x2}} \sim I_0^{S_1^{unm}}) + \Delta V_{oc}^{diff} = 559\ mV}$$

Comparing the two approaches to estimate the V_{oc} of a 1cm^2, based on the scaling behavior of the J_0 and the variation of the V_{oc} for different masking conditions, shows a close agreement:

$$\mathbf{V_{oc}^{S_{a-1}} = 559\ mV \sim V_{oc}^{S_{a-2}} = 562 mV}$$

Band diagram simulations to study the selectivity of the MIS contact

Band Diagram Simulations:

Fig. S6 shows the results of band diagram simulations (details in Methods section), which are performed to investigate the influence of different metal work functions (WF) on the inversion of the n-type silicon. For the chosen WFs between 4.6 - 5.6 eV the conduction bands (E_C) and the valence bands (E_V) are plotted. All the Fermi levels (E_F) are set to 0 eV for clarity. The metal next to the adjacent Al_2O_3 is not shown. As can be seen, the WF of the metal determines the extent of the conduction type inversion in the semiconductor. N-type silicon has a WF of around 4.2 eV, hence employing metals with higher WFs reduces the free electron concentration in the n-type silicon, even leading to strong conduction type inversion in the extreme case. For comparison, silicon that is strongly p-type doped (p^+) has a WF of around 5.3 eV. The simulations show that for WFs between 4.6 – 5.2 eV, an increase in the WF leads to increased inversion. Above ~ 5.2 eV on the other hand, the additional inversion with increasing metal WF becomes less pronounced. Besides the logarithmic dependence of the Fermi level position, part of this decreasing sensitivity of the inversion with increasing WF can be ascribed to the intrinsic (low conductivity) a-Si:H. Between 5.2 - 5.6 eV the initial energy difference of the conduction bands (red, violet and blue lines) at the metal - a-Si:H interface falls off over the intrinsic a-Si:H.

In the simulations shown here, no additional fixed charge density (Q_f) of the Al_2O_3 at the metal - a-Si:H interface is assumed. As can be seen from **Fig. S7**, and discussed in detail below, only an additional fixed charge density with very high (negative) Q_f values of around -10^{13} cm^{-2} has a substantial effect for high WF metals, while for low WF metals (<5 eV) Q_f values above -10^{12} cm^{-2} can already substantially improve the inversion.

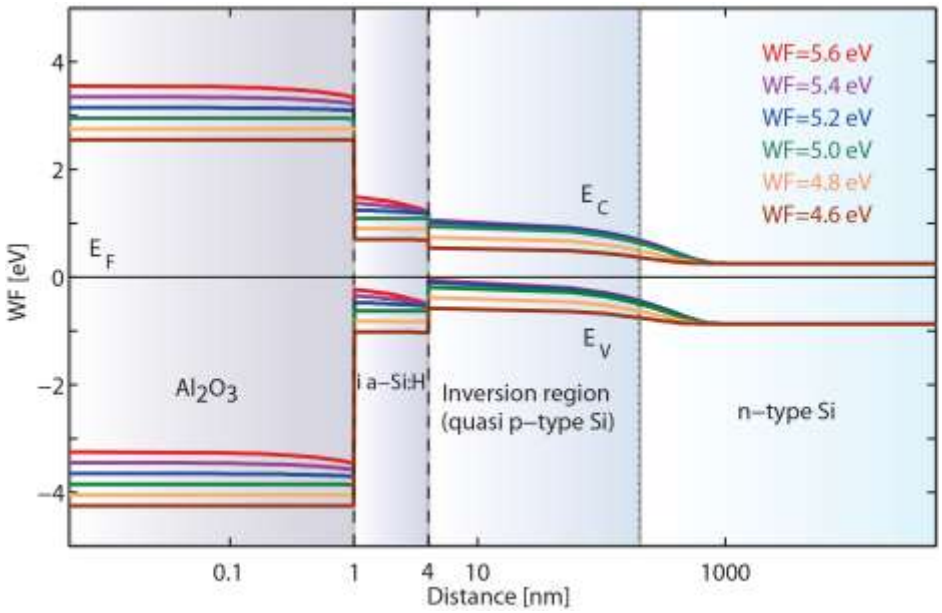

Figure S6: Band diagram simulations showing the influence of the metal work function for the conduction type inversion in silicon. The conduction bands (E_C) are plotted in the upper half (E>0 eV) and the valence bands (E_V) in the lower half of the figure (E<0 eV). For a better overview all the Fermi levels (E_F) are set to 0 eV.

The simulations show that high metal work functions (> 5eV) can lead to strong conduction type inversion in the underlying silicon, the prerequisite for a high V_{oc}. Conversely, any decrease of the effective metal WF will lead to a decrease in the V_{oc}. When corrected for the small illuminated area of our cells compared to the large substrate, the calculated effective V_{oc} is 560 mV. The WF of high purity Pd is reported to be in the range of 5.2 - 5.6 eV, with the exact value being crystal facet dependent.[4] Given our surface passivation scheme and the high purity of the FZ-silicon wafer even a slightly lower work function of Pd, due to trace amounts of impurities, seems insufficient to explain our results (see Fig. S6). A cause for the relatively low V_{oc}, when compared to state-of-the-art silicon solar cells (>700 mV), can be the lowering of the Pd vacuum work function due to the presence of the dielectric Al_2O_3.[5] From developments in the field of complementary-metal-oxide-semiconductor (CMOS) transistors, it is known that Fermi level pinning to a charge neutrality level (CNL) in the dielectric can lower the effective work function of the metal.[5–7] As a result, the effective WF of Pd is lowered to the range of 4.6 - 4.9eV by the dielectric Al_2O_3, which is well below the reference WF of highly doped p-type silicon (~ 5.2 eV). Therefore, other dielectrics, e.g. SiO_2, that cause much weaker Fermi level pinning to the CNL should be employed in future devices. However, when searching for alternatives the stability and passivation properties for ultrathin layers of 1-2 nm have to be kept in mind.

Influence of fixed charge density of Al_2O_3 on extent of inversion layer:

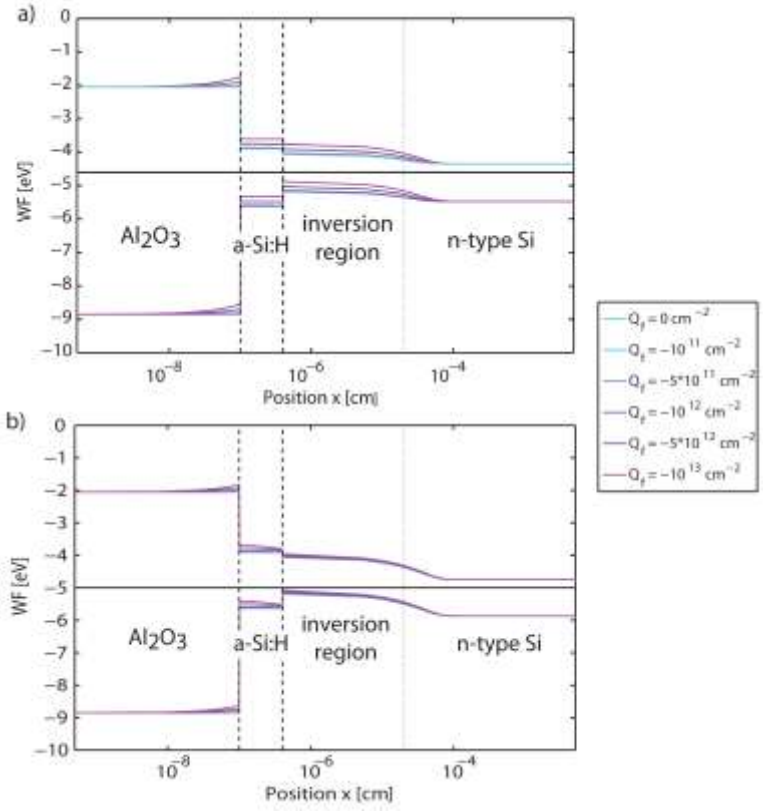

Figure S7: Band diagram simulations showing the influence of a fixed charge density in the Al_2O_3 at a given the metal work function (WF) for the conduction type inversion in the silicon. The conduction bands (E_C), the valence bands (E_V) and the Fermi levels (E_F) are indicated, as well as the boundary regions in between the different employed layers. The metal, positioned left to the Al_2O_3, is not shown. (a) Conduction type inversion for a metal work function of 4.6 eV and a fixed charge density Q_f between 0 cm^{-2} and -10^{13} cm^{-2}. (b) The same as in (a), but with a metal work function of 5 eV.

Al_2O_3 is known to exhibit a fixed charge density at a Al_2O_3-silicon interface, which can lead to electrical passivation of the interface, by repelling minority carriers with the same polarity of the surface charge. This so called *field-effect-passivation* is being used in

solar cells to increase the lifetime of the minority carriers by preventing their diffusion towards recombination active surface/interface sides. For the tunnel and passivation layer employed in this work, consisting of a 1 nm Al_2O_3 and a 3 nm a-Si:H layer, the occurance of a fixed charge density is being debated at the moment.

Therefore**,** we performed band diagram simulations to investigate the effect of a potential fixed charge density on the magnitude of the inversion layer. In principle, a fixed charge denisty could lead to a stronger inversion in MIS type solar cells than given by the difference in work function between the metal and the adjacent semiconductor. **Fig. S7** shows the magnitude of the conduction type inversion for a metal work function of 4.6 eV (6a) and 5 eV (6b) in dependence of a fixed charge density at the Al_2O_3/ a-Si:H interface. The interface charge density Q_f changes between 0 cm^{-2} and -10^{13} cm^{-2}. As can be seen in Fig. S7a, for a metal work function of 4.6 eV the additional fixed charge density can have a very strong effect on the magnitude of the inversion layer. However, as can be seen in Fig. S7b for a higher metal work function of 5 eV, even without a fixed charge density the inversion already reaches the same magnitude than for a work function of 4.6 and a very high fixed charge density of -10^{13} cm^{-2}. Furthermore, any additional fixed charge density only has a relatively smaller effect on the conduction type inversion for a metal work function of 5 eV. This can be understood by the logarithmic dependence of the Fermi level position in the band gap with carrier concentration. Starting with an intrinsic semiconductor, any initial additional carrier concentration will lead to a relatively large change of the Fermi level position. However, any subsequent addition of more charge carriers will lead to a subsequent decrease in the relative change of the Fermi level position. We conclude, that while any additional (negative) fixed charge density could lead to a stronger conduction type inversion (and hence higher V_{oc}) the difference between the metal and the semiconductor work function has a more pronounced effect (compare also to Fig. S6). The reason for that is simply that metals with large work functions exist that can lead to a very strong inversion in the n-type silicon, while fixed charge densities without any additonal metal WF difference would need to reach values for a strong inversion in n-type silicon, that are hard to reach ($>10^{13}$ cm^{-2}). However, any additonal fixed charge density, together with a high metal-semiconductor work function difference is expected to increase the V_{oc}. For the MIS solar cell fabricated for this work, a Pd-Au metal double layer was employed. The Pd interlayer was choosen, due to the somewhat higher work function than Au. The work function of high purity Pd is reported to be in the range of 5.2 - 5.6 eV, depending on the crystal facet. Even taking into account potential impurities due to the evaporation methods used, we expect the metal work function to be high enough to be the dominant reason for the conduction type inversion, with slight modifications due to a potential fixed charge density. Since we observe an effective V_{oc} of around 560 mV, which is substantially lower than for traditional high-efficiency p-n junction solar cells with V_{oc}*'s* > 700 mV, we ascribe, based on the band diagram simulations, a minor importance to the potential fixed charge density in explaining our results. N-type silicon has a work function of around 4.2 eV and p+-type silicon of around 5.2 eV. Therefore, any slight lowering of the metal work function of Pd, due to impurities or the influence of a charge neutrality level (CNL) in the dielectric, as discussed above, will have a much stronger impact on the resulting V_{oc}, than a potential fixed charge density.

We note that a strong inversion in the underlying silicon is not the only factor to consider for high open-circuit voltages in MIS silicon solar cells.

To exclude fabrication induced material degradation as a major cause for the low V_{oc}, lifetime measurements after each fabrication step would be highly desirable. Unfortunately, the specific process sequence (e.g. the initial fabrication of the metalized backside) doesn't allow to track the lifetime with the Sinton lifetime tester. Besides the observed e-beam induced damage of the a-Si:H (Fig. S10), high post-annealing temperatures or other steps known to negatively impact the passivation were avoided.

Furthermore, the selectivity of the contacts will fundamentally determine the degree to which the implied open-circuit voltage (V_{oc}^{imp}) can be translated to the measured V_{oc}.[2,8–10] While it is in general true that a stronger inversion will lead to a higher selectivity, the latter might be limited for conduction type inversion in silicon compared to state of the art diffused junction or SHJ solar cells. However, in the light of the open-ciruit voltages obtained in the past for MIS silicon solar cells, which reached values of 655 mV with inferior passivation layers, we expect the main limiting factor for our solar cells to be the ones discussed above.[11,12]

Lastly, we note, that even given that the energy levels for the electron contact and the hole contact are on the same level as the electron and hole quasi-Fermi levels, i.e. ohmic contacts are established, the actual V_{oc} won't reach the value given by the work function difference, which is about 1 eV for a traditional solar cell. The implied V_{oc}, i.e. the carrier concentration inside the semiconductor, is lowered in a traditional p-n junction solar cell because a considerable amount of charge carriers is moving towards the wrong contact where recombination can take place, i.e. holes move to the electron contact and electrons to the hole contact. That movement is facilitated because of two reasons: First, the minority carrier conductivity in the region close to the contact is not negligible under illumination. Second, the large gradient in the minority carrier Fermi level results in a large driving force for minority carriers towards a majority carrier contact.The large gradient of the minority carrier Fermi level at the majority carrier contact is an inherent characteristic of the energy conversion process, i.e. after the excitation of photogenerated charge carriers, those charge carriers will always experience a driving force towards a lower free energy. This driving force is present at both contacts, but it is larger for the respective minority charge carriers at the contact for the majority charge carriers. Therefore, for a solar cell to function efficiently, the minority charge carrier conductivity close to the majority carrier contact has to be lowered as much as possible.[8]

Optical FDTD simulations of metal nanowire network:

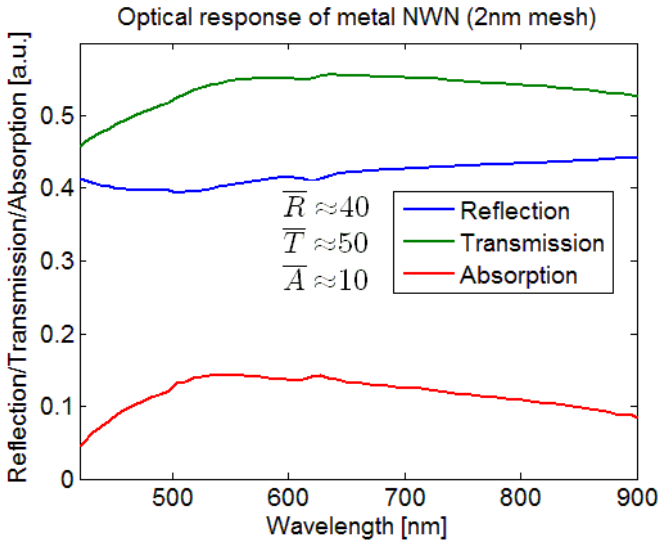

Figure S8: Simulated (FDTD) reflection, transmission and absorption values for metal nanowire network with a thickness of 50 nm (10 nm Pd, 40 nm Au), width of 100 nm, pitch of 1 µm .

Tunnel resistance

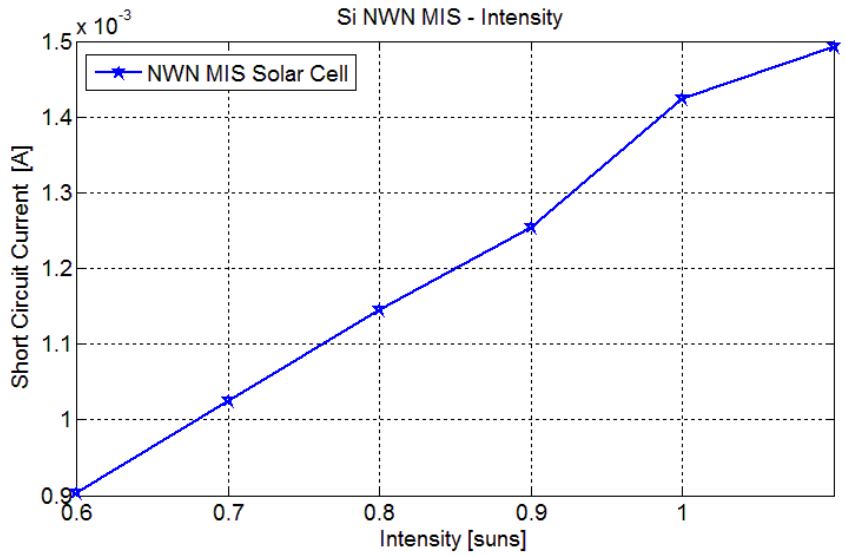

Figure S9: Short-circuit current measurements as a function of illumination intensity. The linear increase of the short-circuit current proves that the contact resistance is not tunnel limited but following a simple ohmic behavior.

Investigation of annealing behavior

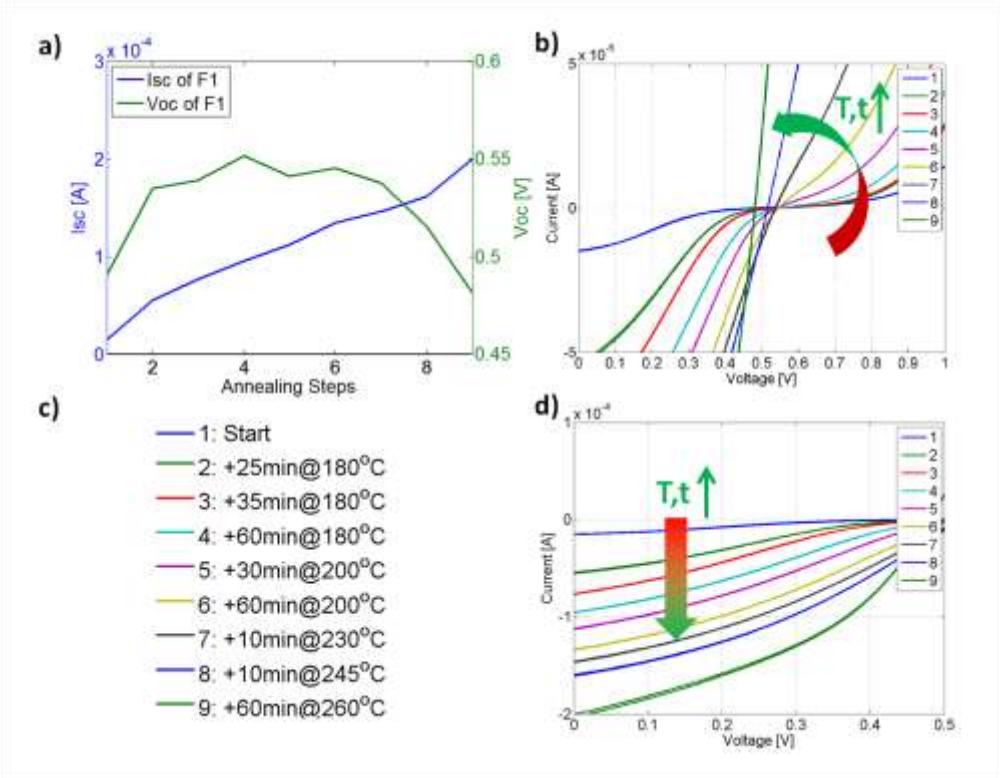

Figure S10: Influence of post-fabrication annealing steps on the I_{sc}, V_{oc} and charge carrier extraction barrier at the interface. The subsequent annealing steps are listed in (c). (a) The measured I_{sc} (blue) and V_{oc} (green) values as a function of the annealing step. As can be seen, the V_{oc} increases before reaching it's maximum for an annealing temperature between 180 - 230 ^{o}C, and an annealing time of around 30 min. The I_{sc} (see also panel d) increases monotonically without reaching a maximum in the range investigated. (b) With increasing annealing temperature and time the s-shaped IV curve and hence the charge-carrier extraction barrier disappears.

After the fabrication of our samples we encounter s-shaped IV curves (**see Fig. S10b)**, which point towards charge carrier extraction barriers at the interface. Electron beam exposure of a-Si:H is known to cause the occurrence of certain defects in the material.[13] As shown by other researchers, [13] and confirmed with our performed annealing experiments, those defects can mostly be removed by annealing the a-Si:H at around 220 °C for 30 min. In that temperature range the s-shaped IV curves disappear and that the measured I_{sc} and V_{oc} values after each subsequent annealing step (see Fig. S10a and d) improve substantially. We reach a maximum for the V_{oc} in the temperature range between 180 - 230 °C and an annealing time of around 30 min. However, the I_{sc} and with it the *FF* (not shown) don't reach a maximum but are monotonically increasing for the temperature and time range investigated. We choose to optimize the annealing conditions with respect to the V_{oc} to be able to make conclusions with respect to the extent of the inversion layer. We note that, while the I_{sc} and *FF* of our solar cells could be better, based on the annealing experiments, we can't exclude the possibility that the V_{oc} value of our cells is reaching a value that is affected by the electron-beam-induced damage in the a-Si:H.

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